Design and Implementation of The High Speed Data Acquisition System Based on DSP and USB

1 Peng Zhao, 2 YaLi Zheng

1 First Author
Yulin University, Yulin, 719000, China, E-mail: zhaopeng9500@126.com

2 Corresponding Author
Mechanized Construction Engineering Company, China Railway NO.5 Engineering Group Co., LTD., Hengyang, China, E-mail: pengzhao1@yeah.net

Abstract
In some areas, such as automatic control, electric measure, spaceflight projects and so on, data acquisition technology is used widely. USB has the characteristics of easy to use, high speed and supporting to cut in or pull out on-line, it becomes a trend in data acquisition technology. To introduce the hardware and firmware design, selecting floating point DSP for microprocessor and Philip Corporation's ISP1581 as USB receiver/transfer control chip. The hardware consists of signal conditioning circuit and USB interface circuit. Based on the analysis and understanding of USB protocol, the firmware is designed by modules and layers. Thus, it has sample structures and clear levels. Different modules and layers have different functions, and the programs convenience revise. At last, to introduce the problems during the debugging are analyzed and summarized, some measures about the system improvement are proposed. Thus, combining USB and DSP is an effective solution to data acquisition with high speed as well as processing and transmitting.

Keywords: USB, Data Acquisition, Floating Point DSP, Firmware, Signal Conditioning Circuit

1. Introduction
With the development of electronic technology, a great progress on high-speed data acquisition and processing technology has been achieved. High-speed data acquisition and processing system are based on DSP both can realize the high-speed collection of signal, and can take analysis and processing to signal in both spatial and spectral domains. It has good development potentiality and competitiveness of market.

The design adopts a new-generation digital signal processor TMS320F28335 from TI. This is a 32-bits floating point DSP. When using floating point DSP in the design, the dynamic range and precision need not be considered. It's easier than fixed-point DSP in software design, and more suitable to use high-level language programming. The maximum sampling bandwidth of ADC module in DSP comes to 12.5MSPS, coordinating with signal conditioning circuit gets larger input voltage range. Selecting DSP for microprocessor control chip, it will be used in many fields. Philip Corporation’s ISP1581 for USB receiver/transfer control chip, which fully complies with the USB Specification Rev.2.0. It provides high-speed USB capacity to microprocessor depends on DSP.

The result of experiments indicated that the signal sampling system has good performance, high precision, and low cost[1-2].

2. Hardware Design
2.1 Signal Conditioning Circuit Design.
TMS320F28335 chip has a 12 bit ADC, the front end for two 8 more than one road switchers and 2 road and sampling/keep implement, constitute a 16 analog input channel, simulation of the channel by automatic control switch hardware, and the simulation results of the conversion channel even order in 16 results in a register; In the 25 MHz clock conversion rate under ADC can reach 80ns; A/D triggered can use software start-up, EVA and EVB, and can convert end or in every time every a conversion end trigger interrupt[3].

These characteristics are concentrated in a chip, making the system has high integration, and the system's stability and anti-jamming ability strengthen. So the design uses the internal A/D converter.
Because F28335 internal A/D converter analog input range is 0V to 3V, in order to make the input voltage range increases, the design uses the input signal conditioning circuit, its function is that makes -10V to 10V voltage after bias adjustment and differential amplifier put the output voltage signal in 0V to 3V. This range fits F28335 inside A/D converter requirements. The input signal conditioning circuit shows in Fig. 1[4]. The integrated operational amplifiers is OPA637, it's a precision high speed ditet operational Amp, gain bandwidth product is 80MHz. The first half part of the circuit is to realize -10V~10V to 0V~10V of translation, the second half part is used to achieve the proportion of voltage conversion, in other words, it is 0V~10V to 0V~3V conversion. The relationship between the input voltage and the output voltage for:

$$U_{OUT} = \frac{R7 \cdot R4}{R5} \cdot \left( \frac{5}{R2} + \frac{Vi}{R1} \right)$$  \hspace{1cm} (1)$$

Among them, R2=R4=5K, R1=R5=10K, R7=3K can reduction for the next type:

$$U_{OUT} = \frac{3}{2} \left( 1 + \frac{Vi}{10} \right)$$  \hspace{1cm} (2)$$

![Input signal conditioning circuit](image)

**Figure 1.** Input signal conditioning circuit

### 2.2. USB Interface Chip Choice.

Currently on the market has a lot of USB interface control chips. According to the function main points have built-in micro controller and no built-in micro controller. Built-in micro controller USB interface chip, are mostly 8051 kernel or enhanced 8051 kernel, due to its processing ability is limited, restricted the transmission rate increase.

ISP1581 belongs to no built-in micro controller interface chip. It has 8K bytes of internal FIFO memory, which is shared among the enabled USB endpoints. At the same time, it's a cost-optimized and feature-optimized Hi-Speed USB peripheral controller, and communicates with the system's microcontroller through a high-speed general-purpose parallel interface. It supports automatic detection of Hi-Speed USB system operation. The internal generic DMA block allows easy integration into data streaming applications. In addition, the various configurations of the DMA block are tailored for mass storage applications. The ISP1581 also incorporates features such as SoftConnect™, a reduced frequency crystal oscillator and integrated termination resistors. These features allow significant cost savings in system design and easy implementation of advanced USB functionality into PC peripherals.
2.3. ISP1581 Interface Settings.

The Microcontroller Interface allows direct interfacing to most microcontrollers. The interface is configured at power-up via inputs BUS_CONF, MODE1 and MODE0.

BUS_CONF set to 1, ISP1581 for general processor model, in this mode, AD [7:0] is eight the address bus, DATA [15:0] is independent of 16 the data bus. BUS_CONF set to 0, interface for the disconnection of bus model, then AD [7:0] for local microprocessor bus (multiplexed address/data), DATA [15:0] only as the DMA bus use.

If pin MODE0 is set to logic 1, pins RD and WR are the read and write strobes (8051 style). If pin MODE0 is logic 0, pins R/W and DS pins represent the direction and data strobe (Motorola style).

When pin MODE1 is made logic 0, ALE is used to latch the multiplexed address on pins AD[7:0]. If pin MODE1 is set to logic 1, A0 is used to indicate address or data. Pin MODE1 is only used in Split Bus mode: in Generic Processor mode it must be tied to logic 1.

The Microcontroller Handler allows the external microcontroller to access the registerrset in the Philips SIE as well as the DMA Handler. The initialization of the DMA configuration is done via the Microcontroller Handler.

This interface design selects the general processor mode, MODE0 is set to logic 1, in other words, reading and writing strobe signal is RD and WR.

2.4. ISP1581 and TMS320F28335 Interface Circuit Design.

F28335 external memory interface use 16 data bus, ISP1581 configuration for the 16 of the general data connection modes, so the interface chip can be directly connected. ISP1581 only has 133 memory units (address range from 0x00 to 0x84), using 8-bit address bus, can be connected by F28335 address bus low eight. The pins XZCS0 from F28335 connects with the pins CS. Compared with F28335, ISP1581 is a low speed equipment, so the READY interface signal is used in the application.

F28335 has rich I/O points [5], so it is very convenient to connect with ISP1581. In the design, the choice of the F28335 GPIO13 to produce ISP1581 reset signal. When ISP1581 need to reset, it produces a width about 500us low level pulse. Choosing the GPIO61 and GPIO58 to control EOT and WAKEUP to execute corresponding function. Specific circuit as shown in Fig. 2.
2.5. ISP1581 Power Supply Circuit Design.

The ISP1581 can be powered from 3.3V or 5.0V. If the ISP1581 is powered from VCC=5.0V, an integrated voltage regulator provides a 3.3V supply voltage for the internal logic and the USB transceiver.

The ISP1581 can also be operated from VCC=3.3V. In this case, the internal regulator is disabled and all the supply pins are connected to VCC.

Considering the ISP1581 chip power consumption and fever problem, this design directly use the 3.3V power supply. For connection details as shown in Fig. 3.

3. Firmware Design

3.1. Firmware Structure.

USB is a host-slave Architecture, equipment can't start any transmission process, it can only respond to the request of the host. In this structure, firmware always have been waiting for orders, according to host's requirements to execute the corresponding program. The whole program design according to the modules and stratification mechanism, Thus, it has sample structures and clearer levels[6]. Different modules and layers have different functions, and the programs convenience revise [7]. The firmware structure and data flow as shown in Fig. 4[8].
In the firmware, hardware abstraction layer complete the communication between F28335 and ISP1581; Command interface contains USB command and status register, in order to visit ISP1581 register and the data of port; USB standard request processing through the port 0 transmission, and complete the host enumeration equipment task; Vendor-specific device request is used to get the firmware version and read data from equipment; An interrupt service routine is used to get data from ISP1581 internal RAM, and store in DSP to make corresponding processing[9]. It also establishing the correct event marks to inform the main program for processing.

### 3.2. Main program design.

The main program to cooperate with each subroutine work and further processing. The flow chart as shown in Fig. 5.

Main body part is infinite circulation, used to cycle inquires sign. For example some request processing, fill data sign and so on. Once mark effective, it into the corresponding subprogram for processing.

### 4. System Debugging and Analysis of the Problems

#### 4.1. System Debugging.

Using BusHound5.0 tests acquisition speed, BusHound5.0 debugging software is a serial bus protocol analysis software, which developed by Perisoft company. It can capture all kinds of control information and data from host, and display the time of the capture and provide a way to test USB.

The actual test using 8K bytes as test block. When the test is completed, BusHound detection to have time is about 750 us. Calculation of data transmission speed is about 9.3 MB/S. BusHound testing interface as shown in Fig. 6[10].
Figure 5. USB main program flow chart

Figure 6. BusHound testing interface

After power up system can't work normally. This phenomenon is that Using USB power supply, the current is not more than 500 mA. If all the power-consumption of the collection system more than 500mA, it cannot use the USB power supply.

ISP1581's temperature rise. This phenomenon is that ISP1581 have two kinds of power supply mode, one kind is + 5.0V power supply, the other kind is 3.3V power supply. And use 3.3V power supply, the inside integrated voltage regulator don't work. Which can significantly reduce the chip calorific value.

Running firmware and loading driver program successfully, but getting wrong data. This phenomenon is to visit ISP1581 make error about time series [11]. For the ISP1581 read operation, the lead time of the minimum value is 0ns. It required effective less time is 15ns, the minimum follow time is 5ns. For write operation, the lead time of the minimum value is 0ns, data valid time minimum 26ns, the minimum follow time is 15ns. For TMS320F2812, choosing the highest 150 MHz clock, then each clock cycle is 6.67ns, the comparison of the ISP1581 timing parameters: the minimum time of leading stage is 0ns, effective stage of the minimum time is 26ns, the minimum follow time is 5ns. For a certain time allowance, actually choice leading stage as a clock cycle (6.67 ns), effective stage as five clock cycle (33.33 ns), follow the stage as three clock cycle (20ns).

5. Conclusion

Through the principle analysis about data acquisition system of the USB interface control chip ISP1581, and discuss about the design of ISP1581 and TMS320F2812, and the problems in the process of debugging is summarized. Selecting general processor of ISP1581. when the input clock of TMS320F2835 is 30 MHz (5 times the frequency of internal), the sampling rate as high as 72.8 Mbps. But compared with the maximum speed 200 Mbps of ISP1581 also has a very big disparity. If you want to improve sampling rate, on the one hand, can use ISP1581 DMA work way and choose processing speed higher DSP; On the other hand, in the firmware programming, does not affect the time series, try to reduce software delays. USB depends on its distinct characteristics to combine with DSP high-speed data processing ability, which is the trend of data collection technology development, has broad application prospects.

6. Acknowledgements

Introducing high-level talents program of Yulin University(11GK55).

7. References


