

FM Stereo Receiver Based on Software-Defined Radio

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Abstract

The paper proposes the FM stereo receiver based on Software-defined Radio by FPGA devices, according to the theories of multi-rate digital signal processing and switching means FM stereo decoding. Through the extraction and half-band filter to achieve down-sampling, the digital phase-locked loop extracted pilot signals and achieve the stereo decoding based sub-carrier switch signal. This article simulates the performance of the receiver in MATLAB Simulink environment and FPGA emulation mode. The simulate results and Signal TAP waveforms show that the method can effectively achieve the FM stereo demodulation. The receiver using common quadrature architecture can combine with other modes demodulation, so it has a high value and broad application prospects.

Keywords: Software-defined radio, Phase-locked loop, FPGA

1. Introduction

With rapid development of communication technology and application, various communication products and standards are plenty, thus in the application of the wireless communication [1, 2], electronic warfare systems [3], the broadband wireless receiver is necessary to meet the range from dozens of M, hundreds of M to several GHz spectrum with different communication standard receiving requirements[4].

Broadband wireless receiver is adept the software defined radio [5, 16] structure, and it can realize receivers for the different communication standards in unity hardware platform.

There are basically three type of analog modulation schemes the amplitude modulation, the Frequency modulation and the phase modulation [6]. Prior to 1960, all transmission systems were analog. Today, typical analog transmissions are the signals we hear on AM and FM radio and what we see (and hear) on television [7]. In an effort to create a realistic sound presentation from recorded music, the FM stereo technique is applied to the radio, cinema and television [8].

FM stereo is widely used in vehicular transceiver[9], mobile communication system[10] and so on, and FM stereo receiving is often used in broadband wireless receiver, so the paper research FM stereo receiver based on software defined radio.

FM stereo signal consist of the main signal (L channel + R channel) and the vice-pilot signal (L channel-R channel). Usually be switch mode switching signal received by the 38kHz stereo decoder output, 38KHz subcarrier negative peak and positive peak moment of the stereo signal corresponding to the L and R channel signals. This approach is the key to accurately extract the pilot signal (19KHz), resulting in switching signal (38KHz). FM stereo reception may be discrete components circuit simulation [11], can also be integrated to achieve [12], or by the DSP and FM stereo decoder chip to achieve [9].

This article describes the FM stereo receiver in the FPGA to achieve FM demodulation and stereo decoding, no stereo decoder chip for analog demodulation and discrete components required, and therefore more simple hardware structure, and because the use of software radio architecture in a unified hardware platform for a variety of modulation demodulation. Section II describes the FM stereo

receiver FM stereo decoder and detail design. Section III shows the MATLAB Simulink simulation results. Section IV gives the FPGA design and compiled the simulation results.

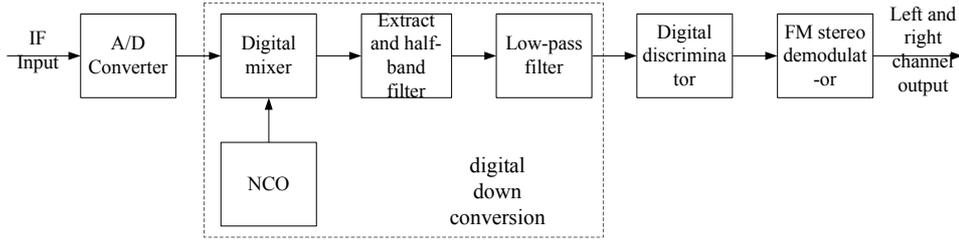


Figure 1. FM stereo demodulator block diagram

2. FM Stereo Receiver

The Software Radios Receiver's A/D converter closer to front, its versatility and flexibility as possible. But direct RF sampling will often result in high hardware cost, then we can frequency (IF) input for A/D sampling. Many commercial communication systems IF carrier is 21.4MHZ or 10.7MHZ and A/D converter sampling frequency is 80MHZ, but the FM stereo signal band is less than 200KHZ, therefore, the baseband signal should down-sampling before demodulation, FM stereo demodulator block diagram show in figure 1. IF input signal from the A/D converter into a digital signal, get the baseband signal by digital down conversion, then by the digital frequency discriminator for FM demodulation, finally, the FM stereo decoder to get the left and right channel output signal.

Digital down conversion usually composed of digital mixer, numerically controlled oscillator (NCO) and low-pass filter. As the FM demodulated baseband signal sampling rate required for the lower, so the design needed to extract and half-band filter before low-pass filter. A / D converter output intermediate frequency digital signal going digital mixer with the NCO generates the intermediate frequency carrier, then get I,Q signals, and the signals include baseband signal and Center frequency of the carrier frequency of the high frequency component 2. Then extract and half-band filter for down-sampling, and then by low-pass filter [17] out high frequency components, resulting in I, Q baseband signals.

Digital mixer is the IF digital multiplied with the quadrature signal $\cos(2\pi f_c n)$ and $-\sin(2\pi f_c n)$ respectively, here f_c is the IF carrier.

In order to achieve Integer multiple of decimation filtering, CIC filter(Cascade Integrator-Comb Filter) can be used. CIC filter is widely applied in the multi-rate signal processing and can inhibit the spread spectrum produced by aliasing. As the CIC filter, the more stages the higher the digit expansion, Therefore, this design uses three cascaded CIC filter, The structure shown in Figure 2. I, Q input signals, respectively, by three points after, to extract multiple, then by three differential and gain adjustment, Decimation filtering can be achieved [13].

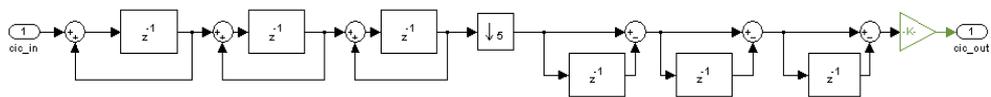


Figure 2. CIC filter

If taking multiple k , for three CIC decimation filter, the gain adjustment factor is k^{-3} . Figure 2 extract multiple $k = 5$, gain adjustment factor for the $1/125$, it can be approximated by $1/128$, thereby to achieve the gain adjustment by move 7 right, after CIC decimation filtering, the sampling rate is $80M/5 = 16MHz$.

The CIC extract the signal after the half-band filter, down-sampling can be achieved. Half-band filter can be used two cascaded half-band filter to achieve 4 times. Make two half-band filter HB1 and HB2, The coefficient as shown in Table 1. Two half-band filter after the sampling rate is $16M/4 = 4MHz$.

Table 1. Extract filter coefficient

coefficient	HB1	HB2
C0	-0.031303406	0.005929947
C1	0.000000000	0.000000000
C2	0.281280518	-0.049036026
C3	0.499954244	0.000000000
C4	0.281280518	0.29309082
C5	0.000000000	0.499969482
C6	-0.031303406	0.29309082
C7		0.000000000
C8		-0.049036026
C9		0.000000000
C10		0.005929947

Down-sampling the signal after the low-pass filtered, can be obtained I, Q baseband signals. Low-pass filter sampling frequency is 4MHz, Pass band is 200KHz, the tap coefficients for 80 bands.

Obviously, the obtained I, Q baseband signals' digital down-conversion meet the general structure quadrature demodulator, the other part of the analog, digital demodulation method (such as AM, PSK, QAM, ASK, etc.) can be shared [14].

3. Digital frequency discriminator

Digital baseband signal to the frequency discriminator can achieve FM demodulation. To simplify the arithmetic operations, can usually be a small angle approximation of the difference calculation.

$$f(n) = X_I(n-1)X_Q(n) - X_I(n)X_Q(n-1) \quad (1)$$

Where $f(n)$ is the frequency of time n , respectively, $X_I(n-1), X_I(n)$ are $n-1$ and n the time of I baseband signal, $X_Q(n-1), X_Q(n)$ are $n-1$ and n the time of Q baseband signal [4]. The structure is shown in Figure 3.

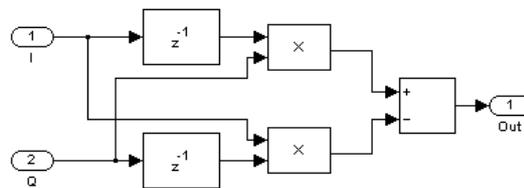


Figure 3. Frequency discriminator

4. FM stereo decoding

After digital frequency discrimination, decoding a stereo signal can get the stereo left and right channel output signal, the structure shown in Figure 4. FM stereo signal is multiplied with the 19KHz,

attained the phase error by loop filter, and the pilot can be extracted by the NCO. Pilot signal from the 19KHz frequency can obtained sub-carrier 38KHz by 2 octave, then by comparison to determine the negative, positive peak time, take the appropriate time of the FM stereo signal and attain the left and right channel signals.

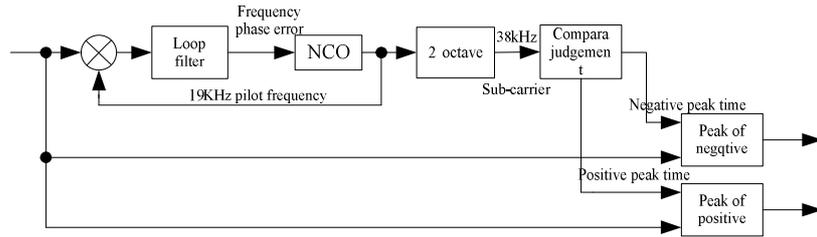


Figure 4. FM stereo demodulate

Loop filter is not only the role of low-pass filter, but played a decisive role in the performance of the loop. The design has adept the second-order loop [15], and the structure shown in Figure 5.

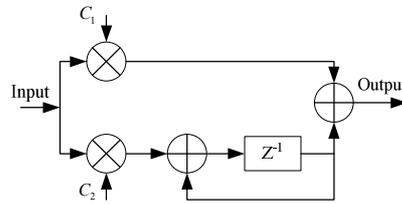


Figure 5. second-order loop filter

Figure in part the product of the coefficients C_1 and coefficients C_2 of integral part of the control loop of the phase tracking and frequency tracking performance, its value is:

$$\begin{cases} C_1 = \frac{2\xi\omega_n T}{K_d} \\ C_2 = \frac{(\omega_n T)^2}{K_d} \end{cases} \quad (2)$$

Where ξ is the loop damping factor, usually take 0.707, ω_n is the loop damping oscillation frequency, T is the NCO frequency word update cycle, K_d is the loop gain.

5. FPGA design

The FPGA designs of FM stereo modulation and demodulation are shown as below. In figure 6, 's_left' and 's_right' are left-channel and right-channel signals of source respectively, 'FM_mod' means FM modulation output, 'sel_left' and 'sel_right' denote minimum-time and maximum-time of the subcarrier respectively, 'Fc38k' is subcarrier signal, 'pfErr_19k' is the phase error of 19kHz pilot signal, and 'left' and 'right' are left-channel and right-channel decoded output respectively. Wherein, 'clk_base' denotes the 4MHz clock signal of down_convert output data.

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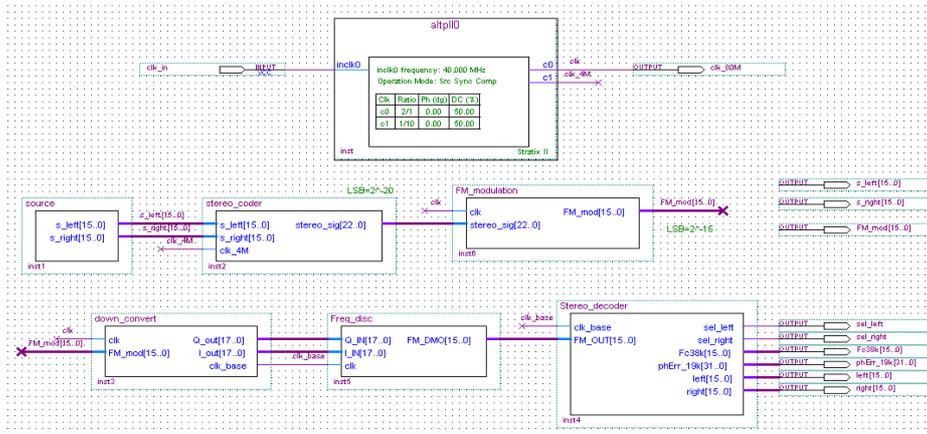


Figure 6. FM stereo modulation and demodulation

In figure 7, the module 'NCO38k' and 'NCO19k' output the subcarrier and pilot signals respectively, and 'stereo_sig' means the output of stereo coder. In figure 8, the module 'plus_c1', 'plus_c2', and 'lpm_add_sub5' make up loop filter, 'ra' means phase error of pilot signal, 'Fc19k' denotes 19kHz pilot signal, 'rc' indicates the subcarrier signal, 's_r' and 's_l' are the outputs of the maximum and minimum comparator respectively.

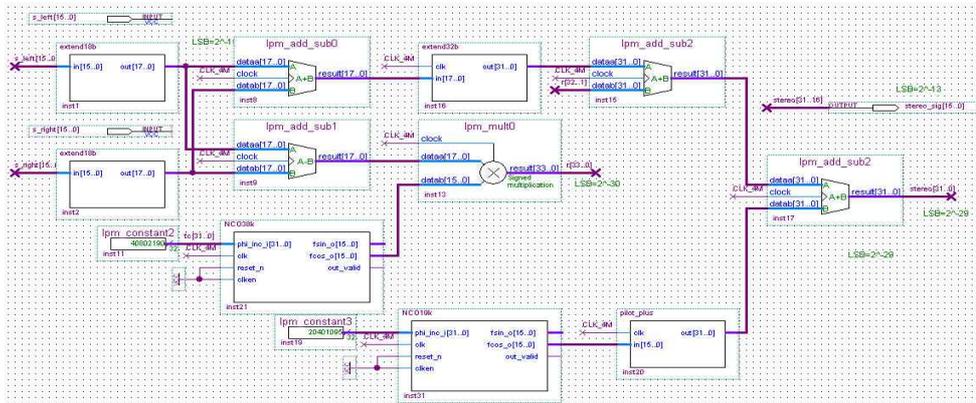


Figure 7. Stereo coder

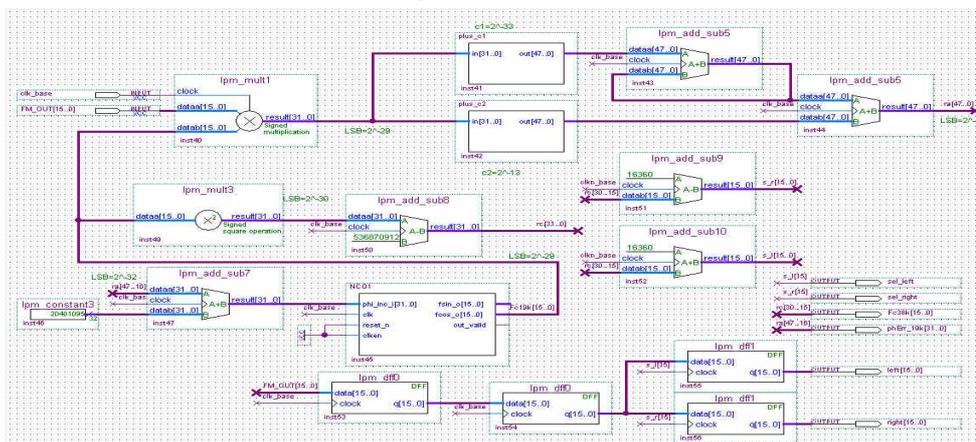


Figure 8. Stereo decoder

An Altera's StratixII chip EP2S180F1020C5 is adopted, FM stereo modulation reconciliation menstruation compilation occupies 21% of logic cells, memory cells 28%. Figure 10 is a FM stereo modulation and demodulation of the Signal TAP waveforms. The waveform graph from top to bottom, respectively: Left channel output, Right channel output, Left channel input, Right channel input, 38KHz subcarrier signal, subcarrier take peak of negative, subcarrier take peak of positive, FM demodulation signal, FM stereo synthesized signal. Left and right channel signals's frequencies are 4.75KHz and 1KHz respectively.

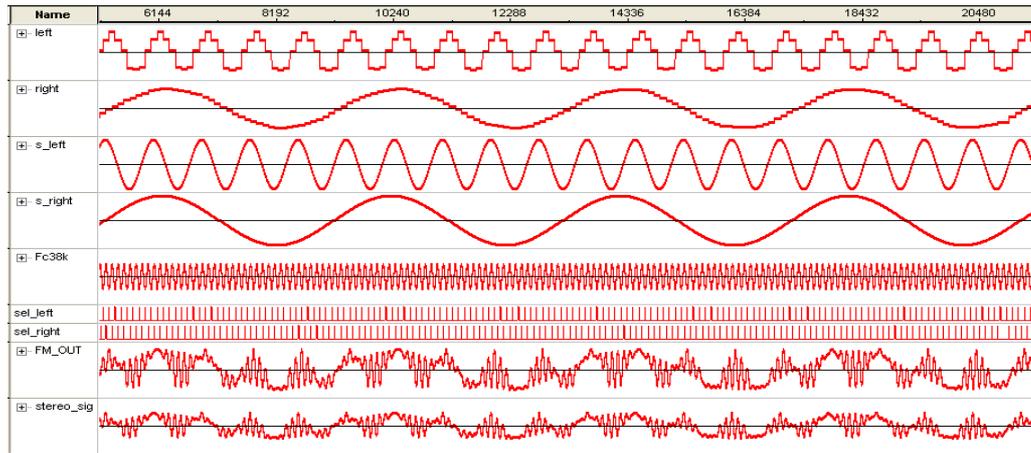


Figure 9. FM stereo modulation and demodulation signal TAP waveform

The figure shows, the waveforms of FM demodulator output and modulation terminal FM stereo signal synthesis are same, left and right channel output waveform with the same input signal. As the left and right channel output is the peak time of the corresponding subcarrier stereo signal, equivalent to a sampling frequency of 38KHz, The left and right channel input sampling frequency of 4MHz, then the left and right output waveforms have obvious sampling distortion compare with the input waveforms.

6. Conclusion

The paper have Proposed software-based radio FM stereo demodulation method based on the multi-rate sampling and switching system FM stereo decoding principle. The Simulink simulation and the FPGA waveform show that the method can effectively achieve the FM stereo demodulation. This demodulation method using general quadrature demodulator structure can be easily combined in a common software radio receiver, resulting in a unified hardware platform to achieve a variety of ways demodulation, and thus has a high value and wide application.

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