Integrated LTSSM (Link Training & Status State Machine) and MAC Layer of USB 3.0 Device for Reliable SuperSpeed Data Transactions

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Abstract

USB (Universal Serial Bus) is the current generation of computer peripherals widely used transmission interface. User applications demand a higher performance connection between the PC and other increasingly sophisticated peripherals. USB 3.0 enables more demanding applications compared to its earlier interfaces – Fast Speed USB 1.1 (12 Mbps) and High Speed USB 2.0 (480 Mbps), because of its high bandwidth (Super Speed 4.8Gbps), efficient power management scheme and reliable data flow control. In this research we have extended our previous work and developed a synthesizable hardware of LTSSM (Link Training and Transition State Machine) for ensuring the reliable USB link for data transfer and efficient power management to reduce any power wasting conditions. We have integrated LTSSM with previously developed USB 3.0 MAC layer controller according to the constraints specified by Intel Corporation in its USB 3.0 specifications sheet. This implementation meets the required constraints and ensures the data rate of at least 4.5 Gbps.

Keywords: USB 3.0, LTSSM, Link Training, Power Management, Error Recovery, MAC layer, PHY Layer Controller.

1. Introduction

The USB 3.0 architecture utilizes very efficient and productive algorithms for maintaining reliable link, highly optimized power consumption and extremely fast and flawless data transfer rate. The Link Training Status State Machine has been employed as the foremost workhorse in these regards. Its functions and provisions contribute matchlessly towards the “super speed” high class performance, delivered by USB 3.0. The LTSSM tunes and trains the USB link for reliable data transfer. It also implements various algorithms for link’s reliability maintenance and is also responsible to recover the link from any errors as may arise. It also plays key role in power management by greatly reducing link’s power consumption and nullifying any conditions that waste power. The LTSSM also performs operations for making the link ready for data transaction in the very beginning when the device is plugged in. Hence LTSSM is the “DATA FLOW GATEWAY CONTROL” for the device. This is the extended research work of [1] in which we developed a MAC Layer of USB 3.0 device. The complete PHY Layer controller along with its interface with other layers is presented in [2].

![Figure 1. Placement of LTSSM and its interfaces with other layers in USB 3.0 device.](image-url)
The core responsibilities of the LTSSM includes:
- Link Training & Initialization
- Power Management
- Error Recovery

The LTSSM communicates and coordinates with almost all the layers of the device namely the PHY, the MAC, the link layer and also the master controller. A pictorial representation of the placement and interconnection of LTSSM with other layers is shown in Figure 1.

2. LTSSM Interfaces

The layers that LTSSM shares signals with are, namely the PHY layer, the MAC layer, the Data Link Layer (DLL) and the master controller. The LTSSM must inform all the layers before opening or closing the gates for data transaction so as to save the device from unnecessary resending or loss of data. Each signal has its own significance and functionality. These signals have been designed up to the USB 3.0 specification’s directions and requirements.

2.1. LTSSM – MAC Layer Interface

The MAC layer acts as an interface between the PHY and LTSSM. It processes signals coming from the LTSSM and correspondingly transmits the appropriate signals to the PHY and vice versa. It also signals other layers about those signals if needed. These signals are needed for a variety of operations like receiver detection, power management and LFPS reception and sending. The MAC-LTSSM interfacing signals have already been defined while developing MAC layer controller [1]. These interfacing signals are reproduced here (Figure. 2) for the convenience and described with their direction and purpose in Table 1. The signals described as inputs are received by LTSSM and those described as outputs are driven by it.

![LTSSM – MAC I/O interface signals](image)

**Figure 2.** LTSSM – MAC I/O interface signals.

2.2. LTSSM – PHY Layer Interface

The LTSSM also shares some direct signals with the PHY layer where MAC’s interception is not necessary and might overload MAC with extra tasks. These signals enable the LTSSM to control the PHY directly when MAC or other layers are inactive for the purpose of its own transactions, thereby reducing device’s power consumption and increasing the efficiency. Such needs arise during link training and error recovery. The LTSSM also shares a power control signal with the master controller of USB 3.0 device to put it into lower power states where it can disable its components for more power saving. Figure 3 and Table 2 describes the communication interface and their description respectively. The signals described as inputs are received by LTSSM and those described as outputs are driven by it.
Table 1: LTSSM – MAC I/O Interface signals’ description.

<table>
<thead>
<tr>
<th>Name</th>
<th>Direction</th>
<th>Active Level</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[1:0]PowerDownLTSSM</td>
<td>OUT</td>
<td>N/A</td>
<td>Instruction for MAC to take PHY chip into the Power State mentioned by LTSSM.</td>
</tr>
<tr>
<td>transmit_LFPS</td>
<td>OUT</td>
<td>High</td>
<td>Instruction for MAC to transmit Low Frequency Periodic Signaling (LFPS) when the PHY is in P1, P2 or P3 state.</td>
</tr>
<tr>
<td>transmit</td>
<td>OUT</td>
<td>High</td>
<td>Instruction for MAC to begin transmission operation followed by the proper protocols.</td>
</tr>
<tr>
<td>receiver_DO</td>
<td>OUT</td>
<td>High</td>
<td>Instruction for MAC to do receiver detection operation.</td>
</tr>
<tr>
<td>[2:0]Rx_status_2LTSSM</td>
<td>IN</td>
<td>N/A</td>
<td>Sends encoded receiver status to LTSSM.</td>
</tr>
<tr>
<td>LTSSM_phy_status</td>
<td>IN</td>
<td>High</td>
<td>Informs LTSSM the completion of several PHY functions including power management, state transitions, rate change, and receiver detection.</td>
</tr>
<tr>
<td>do_rx_termination</td>
<td>OUT</td>
<td>High</td>
<td>Controls the presence of receiver terminations commanded by LTSSM.</td>
</tr>
<tr>
<td>VBUS</td>
<td>IN</td>
<td>High</td>
<td>Indicates the presence of VBUS to LTSSM.</td>
</tr>
<tr>
<td>LFPS_detected</td>
<td>IN</td>
<td>High</td>
<td>Indicates LTSSM that Low Frequency Periodic Signaling (LFPS) is being detected.</td>
</tr>
</tbody>
</table>

Figure 3. LTSSM – PHY I/O interface signals.

Table 2: LTSSM – PHY I/O interface signals’ description.

<table>
<thead>
<tr>
<th>Name</th>
<th>Direction</th>
<th>Active Level</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX [31:0]</td>
<td>OUT</td>
<td>N/A</td>
<td>Used to send 32-bit data to the host when needed</td>
</tr>
<tr>
<td>TX_K [3:0]</td>
<td>OUT</td>
<td>N/A</td>
<td>Used to send 4-bit data K word to the host in accordance with the “Tx” signal.</td>
</tr>
<tr>
<td>RX [31:0]</td>
<td>IN</td>
<td>N/A</td>
<td>Used to receive 32-bit data to the host when needed</td>
</tr>
<tr>
<td>RX_K [3:0]</td>
<td>IN</td>
<td>N/A</td>
<td>Used to receive 4-bit data K word to the host in accordance with the “Rx” signal.</td>
</tr>
<tr>
<td>RX_VALID</td>
<td>IN</td>
<td>High</td>
<td>Set by host to signal valid data reception</td>
</tr>
<tr>
<td>RX_EQ_TRAIN</td>
<td>OUT</td>
<td>High</td>
<td>Used to direct the PHY to bypass normal operations and perform receiver equalization</td>
</tr>
<tr>
<td>RESET_B</td>
<td>IN</td>
<td>High</td>
<td>Used to reset the device registers and buffers</td>
</tr>
<tr>
<td>CLK</td>
<td>IN</td>
<td>N/A</td>
<td>Provided by PHY as the operational clock frequency</td>
</tr>
<tr>
<td>TX_ELEC_IDLE</td>
<td>OUT</td>
<td>High</td>
<td>Set by LTSSM to start or stop data transaction</td>
</tr>
</tbody>
</table>
2.3. LTSSM – Link Layer Interface

The Data Link layer frequently needs to communicate with the LTSSM during various operations. It signals the LTSSM about the emergence of any link error that must drive the LTSSM into error recovery procedures. The link layer also needs to tell the LTSSM about any link power management commands from the host that might need LTSSM’s intervention since almost all the power optimization is catered by the LTSSM.

3. An overview of the LTSSM state machine

The state machine of LTSSM is specified with 12 main states that carry out these responsibilities. Four of these states are solely for power management. These four states are named as U0, U1, U2, and U3 in [3], whereas they are termed as P0, P1, P2 and P3 in [4]. We’ll use the later case throughout this article since because the same terminology has been used in [1] and [2]. The reader should keep this thing in mind that the power states naming convention, U0-U3, is used in the domain of LTSSM whereas, P0-P3, is used in MAC Layer’s domain, however they are interchangeable.

These four states provide different levels of energy saving schemes. P0 being the active most state having all the modules in the device active, while P3 being the most dormant state with maximum power saving facilities, though at a higher latency rate. The P1, and P2 are intermediate power states that provide certain selective levels of power saving. Compared with P1, P2 allows for further power saving opportunities with a penalty of increased exit latency. P3 is a link suspended state where aggressive powers saving opportunities are possible. The USB 3.0 has been designed for maximum power saving, rendering the device completely inactive or “sleeping” when not in use. This enhances up time for portable devices e.g. laptops etc.

There are two link training and initialization states namely RX_DETECT and POLLING. The RX_DETECT state is designated for the link’s far end receiver detection whereas POLLING is mainly reserved for link training and receiver aligning. RX_DETECT represents the initial power-on link state where a port is attempting to determine if its SuperSpeed link partner is present. POLLING is a link state that is defined for the two link partners to have their SuperSpeed transmitters and receivers trained, synchronized, and ready for packet transfer.

The error recovery states are RECOVERY and COMPLIANCE. These states are entered in case of any sort of mismatching of synchronization or malfunctioning. Another state is LOOPBACK which is used as a ping to check the reliability and operation of the receiver and transmitter. Next come two states that result in case of recovery failure or when the device is disconnected. These states are SS_DISABLED which is entered when device is completely rendered inactive or is disconnected, and the SS_INACTIVE state which is entered when the device cannot operate in “super speed” mode. In the last comes the HOT RESET mode which is entered when the host desires to reset the device. The brief description of LTSSM states are described in the following sub sections.

3.1. SS_DISABLED

It is a state where a port’s SuperSpeed connectivity is disabled with its receiver termination removed. SS_Disabled is also a logical power-off state for a self-powered USB device. The port does not receive or transmit any USB signals in this mode. Only VBUS is detectable in this state.

3.2. SS_INACTIVE

This mode is entered as a result of far end receiver removal or other non-recoverable errors. During SS_Inactive, a port periodically performs far-end link partner detection. If a link partner is not detected, the device returns back to RX_DETECT, otherwise the link stays in SS_Inactive state until software intervention is made by issuing a warm reset.
3.3. RX_DETECT

This is the “Power On” state of the LTSSM for a USB 3.0 device that is entered after Power On Reset and Warm Reset, and is used to detect the impedance of far-end receiver. A port performs the far-end receiver termination detection periodically during RX_DETECT operation. If the link partner is detected, then LTSSM makes a transition to the link training state called POLLING. Otherwise it remains in RX_DETECT.

3.4. POLLING

The Polling state is meant for link training and alignment of receiver transmitters of link partners. Once trained, they can then reliably transfer SuperSpeed data. During Polling, a handshake takes place between the two partner ports via successful exchange of certain data sets using LFPS signals. This results in the achievement of bit phase lock, symbol alignment and receiver equalization. On physical layer level, partners’ D.C operating point and electrical synchronization is achieved during this state.

The LFPS signals used during this state are TSEQ, TS1 and TS2. These are low frequency low power signals useful for training and error recovery. The TSEQ, TS1 and TS2 are 32, 16 and 16 bytes ordered data sets respectively. These signals are collectively referred to as POLLING.LFPS signals. Their exact values and timings can be found in the USB 3.0 Specification [3].

For successful completion of the handshake, more than 50,000 sets of TSEQ training sequences are exchanged to perform receiver equalization. This is followed by the exchange of TS1 ordered sets for the purpose of data reliability assurance. Up to 16 sets of identical TS1 sequences are required to be exchanged by both partners for a successful TS1 handshake. Next, TS2 ordered sets are exchanged which contain different configuration settings. These configurations are decoded and the next state is decided whether it is to be the active P0 state or some other possible transition.

Upon successful accomplishment of all these steps the LTSSM is ready to put the USB link in SuperSpeed packet transfer mode that is P0, where all types of packet transfer is available and the link is fully active.

3.5. P0 – Link active

P0 is the normal operational state where packets can be transmitted and received. All layers are active and working in this state. This state consumes maximum power so this mode is sustained only as long as SuperSpeed packet transfer continues or is expected to execute within a stipulated time out period, after which, this state exits to other low power states for power saving.

3.6. P1 – Link Idle with fast exit

P1 is a low power state where no packets are to be transmitted. This mode is “light sleep” so it provides fastest transition back to other states. There are two possibilities of exiting this state. If any packet transfers are needed again within a specified time out period (P2 inactivity timeout), then it moves back to active state, otherwise, it moves to an even lower power mode P2.

3.7. P2 – Link Idle with slow exit

P2 is an even lower power mode that provides even deeper power saving capability but with an increased wake up time. The device goes into “moderate sleep” so it takes bit longer than P1 to wake up. P2 state can make a transition only to P0 state, upon any of the link partners’ initiation, when a packet needs to be transmitted.
3.8. P3 – Link suspended

It is the deepest low power link state where aggressive power saving is provided but its exit latency is much higher than other two modes. The device goes into “deep sleep” so it takes the longest to awake the device. The host orders the device’s LTSSM to transition to this state when the host sees that link operation will not be needed for long and it can be put into dormant mode.

3.9. Recovery

The Recovery link state is entered to retrain the link after undergoing a serious error, or to perform Hot Reset. The process of retraining is almost the same as initial training in POLLING. However, in this case only TS1 and TS2 ordered sets are transmitted and not TSEQ.

3.10. Loopback

Loopback is intended for testing the accuracy and compatibility of SuperSpeed receiver and transmitter and also for fault isolation. Loopback includes a bit error rate test (BERT) state machine. Loopback master is the port that starts loopback and slave is the port that replies back.

3.11. Compliance

Compliance Mode is used to test the transmitter for compliance to voltage and timing specifications. Several different test patterns are transmitted during compliance mode, which are designed for tuning different physical parameters of the physical layer. The LTSSM make a transition to RX DETECT from this state upon the issuance of Warm Reset.

3.12. Hot Reset

This mode is used by either the device or the host to reset all registers and timers of both link partners. When the host initiates reset, it transmits TS2 ordered sets with the Reset bit asserted, which is then followed by the device. Once both ports receive the TS2 ordered sets with the Reset bit de-asserted, they exit from Hot Reset and return to U0 after exchanging IDLE symbols.

4. Description of LTSSM’s functionalities

This section describes the functionalities of LTSSM as to what is meant by each of them and how are they executed. It gives an insight of what procedures and protocols that the link follows during each of the following three main functions of LTSSM.

4.1. Link training and initialization

One of the core tasks of the LTSSM is to train and make the USB 3.0 link ready for data transaction. This process starts with the detection of a link partner at the far end of the link in the RX_DETCT state. The detection starts as soon as the partner is plugged in to the bus. Once the far end receiver detection is complete, the LTSSM then starts training the link for synchronizing with the clock frequency and bit locking, in the POLLING state, with the transmission and exchanging of TSEQ, TS1 and TS2. These training sequences contain data bits that are designed to train and align the receivers of two link partners. First of all TSEQ is sent for a specified number of times, then TS1 sequences are sent and received as well since the far end partner is also designed to detect and send back these sequences. Upon a successful handshake of all these link training stages between the link partners, the link is then brought to the active power state, the P0 state. Here it is ready to carry out all SuperSpeed data transmissions and receptions. The block diagram of a link training and initialization process is shown in Figure. 3.
4.2. Power management

The USB 3.0 architecture manages power consumption in a very peculiar and efficient manner, which minimize power drainage from the host as long as possible. P0 is the state where data packets are exchanged at super speed and all other communications are openly made. As soon as this data transfer operation is completed, and there is no more data transfer expected or scheduled, the system immediately puts device into lower power mode, P1. If the link is still idle for a specified time in this period it sweeps to P2 which provides even more power saving. Upon further idle behavior the device is brought into deep sleep or “P3” mode which provides maximum power saving features by turning off even the internal clocks for most modules. The device then stays in this mode until re-triggered by the host. The power management process is pictured in Figure 5.
4.3. Error recovery

The LTSSM, as per the specification is designed to handle and recover from any error states resulting in any link disturbances or other reasons. The RECOVERY state defined in LTSSM is entered whenever the link fails the operation, or faces some errors or miss-matches. This state performs the retraining of the link and then resets the device for retrieval of the data transfer mode that it was formerly in. The COMPLIANCE mode is chiefly meant to check if the receiver and transmitter are in proper alignment. If not, then this mode re-aligns the host and device for proper data transfer. Figure 6 shows a flow procedure of error recovery process.

5. LFPS – Low frequency periodic signals

The LTSSM is also associated with the very useful provision of USB 3.0, which are the low frequency periodic signals (LFPS). These signals are of very low power and perform very important tasks like handshakes, reset generation and device active pinging which enable power saving and even higher speeds. These LFPS signals are characterized on the basis of their timings and repetitions as:

- **POLLING.LFPS** – Used during POLLING state for link training.
- **PING.LFPS** – Used during P1, P2 and COMPLIANCE as keep alive signal.
- **U1/U2_EXIT_LFPS** – Used during P1/P2 to transit to recovery and then to P0.
- **U3_WAKEUP** – Used during P3 to transit to recovery and then to P0.
- **Warm Reset** – Used to reset device registers and counters.

There are also various timers, counters and sequence senders associated with the LTSSM that are constantly utilized for LTSSM’s operations. All these timers work under the reluctances allowed in the specifications. All timeout values must be set to the specified values after PowerOn Reset or Inband Reset.
6. Resource Utilization

The hardware resources (of XILINX Virtex-5 XC5VLX110T device) utilized by LTSSM and MAC layer is summarized in Table 3. Table 4 reveals the combined resource utilization by both of the modules.

<table>
<thead>
<tr>
<th>Module</th>
<th>Resources</th>
<th>Used</th>
<th>Available</th>
<th>Utilization</th>
</tr>
</thead>
<tbody>
<tr>
<td>LTSSM</td>
<td>Register</td>
<td>490</td>
<td>69120</td>
<td>0.7%</td>
</tr>
<tr>
<td></td>
<td>LUT</td>
<td>51</td>
<td>69120</td>
<td>0.07%</td>
</tr>
<tr>
<td></td>
<td>Slice</td>
<td>386</td>
<td>17280</td>
<td>2.2%</td>
</tr>
<tr>
<td>MAC Layer</td>
<td>Register</td>
<td>108</td>
<td>69120</td>
<td>0.15%</td>
</tr>
<tr>
<td></td>
<td>LUT</td>
<td>222</td>
<td>69120</td>
<td>0.32%</td>
</tr>
<tr>
<td></td>
<td>Slice</td>
<td>116</td>
<td>17280</td>
<td>0.67%</td>
</tr>
</tbody>
</table>

Table 4: Total hardware utilized by LTSSM and MAC layer.

<table>
<thead>
<tr>
<th>Resources</th>
<th>Used</th>
<th>Available</th>
<th>Utilization</th>
</tr>
</thead>
<tbody>
<tr>
<td>Register</td>
<td>598</td>
<td>69120</td>
<td>0.86%</td>
</tr>
<tr>
<td>LUT</td>
<td>273</td>
<td>69120</td>
<td>0.39%</td>
</tr>
<tr>
<td>Slice</td>
<td>502</td>
<td>17280</td>
<td>2.9%</td>
</tr>
</tbody>
</table>

It is also evident in table 4 that the enough resources are still available to implement Data Link Layer and Protocol Layer (for details see Fig. 9 of [2]).

7. Functional Verification

The functional verification of the operations and functionality of the LTSSM module have been tested on ModelSim (an HDL simulator by Mentor Graphics) by simulating a host model that actuates and responses in exact manner as does the actual host. The test bench is developed where the host operations have been designed to actuate certain operations like link partner detection and link training. During link partner detection the host model sent exactly same data patterns as would have been expected by actual host. The LTSSM’s response to those actuations has been monitored and verified with the actual specification [3]. It is found that the developed LTSSM behaves in a very accurate way and generates up to spec output signals to all the modules that it is connected to.

Figure 7 shows the simulation timing diagrams of link partner detection process during the RX.DETECT state. As soon as the reset is de-asserted and receiver detection is enabled, the PHY layer signals the presence of a link partner by asserting the “phy_status” signal and at the same time setting the appropriate status at “rx_status” signal. On the next clock cycle, the LTSSM senses this signal and transitions from RX.DETECT state to POLLING state as represented by the “ltssm_cs” register value that changes from 0x25 (RX.DETECT state) to 0x07 (POLLING state), where the link training takes place.

The link training process simulation timing diagram is depicted in Figure 8. The LTSSM begins with the Polling state (“ltssm_cs” register value = 0x07) and starts transmitting TSEQ ordered sets on the “tx” signal. After sometime the host also sends back TSEQ sequences which are received on the “rx” data bus. After this, the TS1 and TS2 ordered sets are transmitted and received simultaneously. Finally upon exchanging certain number of these sequences, the link enters P0 active mode. This mode is depicted by “ltssm_cs” value = 0x00. The “u0” and “transmit” signals are also asserted indicating that SuperSpeed data transfer is now possible. The “ltssm_cs” register’s different values (0x17, 0x27, 0x47 and 0x77) are different sub-states of the Polling state which are used to exchange different ordered sets each. In this way link training and alignment is achieved and the link is made ready to carry out SuperSpeed data transfer.
8. Conclusion and Future Enhancements

As the SuperSpeed USB 3.0 protocols are intended for dual simplex transmission lines, for the sake of parallel transactions, there is an absolute need of having the architecture which support such protocols. We have developed a fully synthesized LTSSM (Link Layer and Transition State Machine) and also interfaced it with previously developed MAC layer. Following the latest USB 3.0 specifications, the designed LTSSM can easily be hooked up with other layers. The functionality of LTSSM is also verified, via simulation, along with integrated MAC layer and Master Controller.
The layered architecture of USB 3.0 communication protocols itself turned out helpful in structuring verification effort to enhance it. The layers can be verified separately with minimal overhead in the test development effort. Link layer and Protocol layer will be developed in future as independent modules. Together with the collaboration of Master Controller, LTSSM and all layers – MAC layer, link layer and protocol layer, a single entity of a USB 3.0 memory device can be developed.

9. Acknowledgment

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10. References


[7]. “Inter-Chip USB Supplement to the USB 2.0 Specification”, Revision 1.0, March 13, 2006.
